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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,743	07/16/2003	Shih-Chung Chou	10112491	8967

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,743	CHOU ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: On page 7, line 10, Applicant discloses that the ion implantation gas is "a gas mixture containing F, such as chlorine gas". The examiner believes applicant intended on reciting fluorine gas rather than chlorine gas.

Appropriate correction is required.

Claim Objections

Claims 1 and 10 are objected to because of the following informalities: In lines 10-11 of claim 1, and lines 11-12 of claim 10, the examiner believes that "ion implanting the top portion of the deep trench to a predetermined angle" should be replaced with –ion implanting the top portion of the deep trench at a predetermined angle--. Appropriate correction is required.

Claim 10 is objected to because of the following informalities: In lines 18-19 of the claim, the examiner believes "the second oxide layer" should be replaced with –the thickness of the second oxide layer—in order to clarify that it is the thickness of the first and second layers that is being compared.

Claim 21 is objected to because of the following informalities: Claim 21 should be dependent on claim 10, rather than claim 1. Claim 21 seems to be a duplicate of claim 9, which is dependent from claim 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the exposed semiconductor substrate" in line 16-17. There is insufficient antecedent basis for this limitation in the claim. The claim as written has no step of exposing the semiconductor substrate. Further, as understood by examiner the substrate would necessarily have an oxide formed on the sidewall during the oxidation step. It appears that the claim lacks a recitation of etching the oxide to expose the substrate.

Further, in lines 4-9 of claim 1, Applicants recite, "the deep trench capacitor having a node dielectric layer and storage node, the node dielectric layer covering a sidewall and a bottom portion between the deep trench and the deep trench capacitor, and the storage node filling the deep trench to a predetermined depth". The examiner notes that the node dielectric layer is part of the deep trench capacitor, and therefore, cannot be formed in between the deep trench and the deep trench capacitor. The examiner believes Applicants intended to recite that the node dielectric layer covers a sidewall and a bottom portion between the deep trench and the storage node of the deep trench capacitor.

Similarly, in lines 4-9 of claim 10, Applicants recite, "the deep trench capacitor having a node dielectric layer and storage node, the node dielectric layer covering a sidewall and a bottom portion between the deep trench and the deep trench capacitor, and the storage node filling the deep trench to a predetermined depth". The examiner notes that the node dielectric layer is part of the deep trench capacitor, and therefore, cannot be formed in between the deep trench and the deep trench capacitor. The examiner believes Applicants intended to recite that the node dielectric layer covers a sidewall and a bottom portion between the deep trench and the storage node of the deep trench capacitor.

Claims 2-9 and 11-21 are rejected under 35 U.S.C. 112, second paragraph for being dependent on rejected claims 1 and 10.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Tews et al. (U.S. Patent No. 6,426,253).

Tews et al. teaches a method for forming a trench capacitor comprising:

providing a semiconductor substrate (100), wherein a deep trench (104) and a deep trench capacitor (see column 8, lines 3-6) are formed therein, the deep trench capacitor having a node dielectric layer (108) and storage node (110), the node dielectric layer covering a sidewall and a bottom portion between the deep trench and the deep trench capacitor, and the storage node filling the deep trench to a predetermined depth;

ion implanting the top portion of the deep trench to a predetermined angle to form an ion doped area on a single sidewall of the semiconductor substrate and the top surface of the deep trench capacitor (see column 6, line 63 through column 7, line 8);

oxidizing the semiconductor substrate to form an oxide layer on the ion doped area (see column 7, lines 8-30);

forming a sidewall layer (130) on the exposed semiconductor substrate using the oxide layer as a mask;

removing the oxide layer (see Figure 11, column 8, lines 1-3);

forming a barrier layer (138) on the sidewall of the deep trench; and

filling a conducting layer (140) in the deep trench.

In re claim 5, Tews et al. disclose the method wherein the material of the sidewall layer (130) is the same as the semiconductor substrate (silicon, see column 7, lines 45-50 and column 6, lines 3-6).

In re claim 6, Tews et al. disclose the method wherein the barrier layer (138) is an oxide or a nitride layer (see column 8, lines 30-37).

In re claim 7, Tews et al. disclose the method wherein the conducting layer (140) is a poly layer (see column 38-43).

In re claim 8, Tews et al. disclose the method wherein the node dielectric layer (108) is a silicon nitride layer (see column 6, lines 39-44).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tews et al. (U.S. Patent No. 6,426,253) in view of Kawai et al. (U.S. Patent No. 6,410,991).

Tews et al. disclose the method as claimed and rejected above, but do not disclose the method wherein the ion source of the ion implantation is a gas mixture containing F, which promotes growth of the oxide layer or the method wherein the gas mixture containing F is fluorine gas. Kawai et al. discloses the method wherein an ion source of the ion implantation for changing the oxidation rate of silicon is a gas mixture containing F and wherein the gas mixture containing F is fluorine gas (see column 6, line 54 through column 7, line 10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the materials of Kawai et al. because as Tews et al. teaches any dopant may be used (see Tews et al. column 6,

lines 63-66) and Kawai et al. teach BCl_3 or F_2 are suitable materials for altering the oxidation rate as need in Tews et al.

Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tews et al. (U.S. Patent No. 6,426,253) in view of Divakaruni et al. (U.S. Patent Appl. 2001/0042880).

In re claim 4, Tews et al. disclose the method as claimed and rejected above, but does not disclose the method wherein the sidewall layer is an epi-silicon layer. Divakaruni et al. disclose the method wherein the sidewall layer is an epi-silicon layer (see paragraph [0031], and [0034]-[0036]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the sidewall layer of epitaxial silicon because as Divakaruni et al. teach the epitaxial silicon allows a natural electrical buried strap connection (see paragraph [0036]).

In re claim 9, Tews et al. disclose the method as claimed and rejected above, but does not disclose the method wherein the storage node is an n+ type doped poly. Divakaruni et al. teach that the storage node is n doped poly (see paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the storage node of Tews et al. with n doped poly because as Divakaruni et al. teach the dopants may be either n or p as the required (see paragraph [0005]).

Allowable Subject Matter

Claims 10-21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the method including the limitations of ion implanting the deep trench top portion at a predetermined angle to form an ion doped area on the semiconductor substrate of the first sidewall and the top surface of the deep trench capacitor, oxidizing the semiconductor substrate to form a first oxide layer on the ion doped area and a second oxide layer on the second sidewall, wherein the thickness of the first oxide layer exceeds the second oxide layer thickness, removing the second oxide layer to expose the semiconductor substrate of the second sidewall of the deep trench, forming a sidewall layer on the second sidewall using the first oxide layer as a mask, conformally forming a first barrier layer on the first sidewall, the sidewall layer, and the deep trench capacitor in combination with the other limitations of independent claim 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk